PATENT ABSTRACTS OF JAPAN

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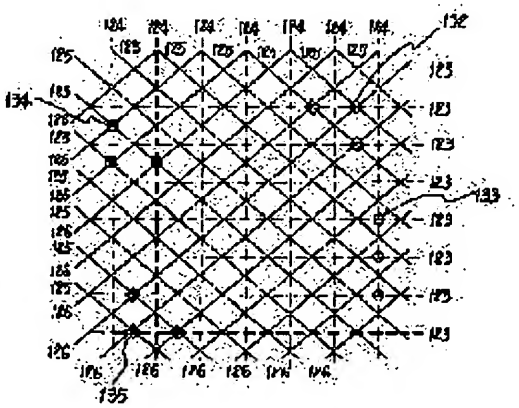
(54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

(57)Abstract:

PURPOSE: To reduce the area of a chip as a whole by a method wherein a wiring region on a hard macro inside a semiconductor chip is made small.

CONSTITUTION: The following are arranged: third-layer interconnections 123 and fourth-layer interconnections 124 which are formed on a hard macro; and fifth-layer interconnections 125 and sixth-layer interconnections 126 which cross them obliquely. In addition, the following are formed: second through holes 132 which connect second-layer interconnections to the thirdlayer interconnections 123; fifth through holes 135 which connect the fifth-layer interconnections 125 to the sixth-layer interconnections 126; fourth through holes 134 which connect the fourth-layer interconnections 124 to the fifth-layer interconnections 125; and third through holes 133 which connect the third-layer interconnections 123 to the fourth-layer interconnections 124. Thereby, a wiring operation can be performed at a shortest distance on the hard macro.



LEGAL STATUS

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CLAIMS

[Claim(s)]
[Claim 1] The hard macro which connected between basic transistor components and was formed using the 1st-layer wiring and the 2nd-layer wiring which were prepared on the semiconductor chip, The 3rd-layer wiring arranged in the longitudinal direction which connects between said hard macroes, The 4th-layer wiring arranged to the lengthwise direction which crosses perpendicularly to said 3rd-layer wiring, and forms a grid, Semiconductor integrated circuit equipment characterized by having the 5th-layer wiring and the 6th-layer wiring which cross aslant, respectively and cross mutually to the 3rd-layer wiring and the 4th-layer wiring of those other than the intersection of said 3rd-layer wiring and the 4th-layer wiring.
[Claim 2] Semiconductor integrated circuit equipment according to claim 1 with which the 5th-layer wiring and the 6th-layer wiring have been arranged on a hard macro.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] Especially this invention relates to wiring between the hard macroes in a chip about semiconductor integrated circuit equipment.
[0002]
[Description of the Prior Art] Generally according to the miniaturization of equipment, and the demand of a system, as for semiconductor integrated circuit equipment, the degree of integration is high every year.
[0003] The 1st-layer wiring 221 arranged in the longitudinal direction on a drawing as conventional semiconductor integrated circuit equipment is shown in drawing 4 , The 3rd-layer wiring 223 which has arranged in the longitudinal direction like the 2nd-layer wiring 222 and the 1st-layer wiring 221 which have been arranged to the lengthwise direction on a drawing, and used the wiring pitch as the 1st-layer wiring [twice] 221 is arranged. The 1st through hole 231 which constitutes the grid of the minimum wiring spacing from the 1st-layer wiring 221 and the 2nd-layer wiring 222, and connects the 1st-layer wiring 221 and the 2nd-layer wiring 222 in the lattice point, It has the 2nd through hole 232 which connects the 2nd-layer wiring 222 and the 3rd-layer wiring 223 in the lattice point to the grid made from the 2nd-layer wiring 222 and the 3rd-layer wiring 223.
[0004] Drawing 5 and drawing 6 are the layout patterns showing the 1st and 2nd examples of conventional semiconductor integrated circuit equipment.
[0005] As shown in drawing 5 and drawing 6 , when it constitutes between the hard macro A formed on LSI chip 11, and the hard macro B using the 1st-layer wiring 221 and the 2nd-layer wiring 222 When making wiring connection from the hard macro A to the hard macro B according to the wiring pitch shown in drawing 4 , since it cannot wire only using the 1st-layer wiring 221 and the 2nd-layer wiring 222, the hard macro B top There are an approach of passing the hard macro B top using the 3rd-layer wiring 223 as shown in drawing 5 , and the wiring approach of using and taking about the 1st-layer wiring 221 and the 2nd-layer wiring 222 in the wiring field 13 around the hard macroes A and B as shown in drawing 6 . The former shown in drawing 5 pulls out the output of the hard macro A using the 2nd-layer wiring 222. Make it connect with the 3rd-layer wiring 223 in the 2nd through hole 232, and the hard macro B top is passed using the 3rd-layer wiring 223. Make it connect with the 2nd-layer wiring 222 after passage in the 2nd through hole 232, make it connect with the 1st-layer wiring 221 using the 1st through hole 231 after that, and it is made to connect with the 2nd-layer wiring 222 using the 1st through hole 231 again, and has composition used as the input of the hard macro B. The latter shown in drawing 6 pulls out the up output of the hard macro A using the 2nd-layer wiring 222. Connect with the 1st-layer wiring 221 using the 1st through hole 231, and it wires to the chip upper left. Connect with the 2nd-layer wiring 222 using the 1st through hole 231, and wiring is delayed to the lower left. It connects with the 1st-layer wiring 221 using the

1st through hole 231 again, connects with the 2nd-layer wiring 222 using the 1st through hole 231 of a degree often, and has composition used as the input of the hard macro B.
[0006]
[Problem(s) to be Solved by the Invention] As shown in drawing 4 , with conventional semiconductor integrated circuit equipment, like the 1st-layer wiring 221 of the longitudinal direction of drawing, the 2nd-layer wiring 222 of the lengthwise direction of drawing, and the 1st-layer wiring 221 The 3rd-layer wiring 223 of the longitudinal direction of drawing, Have the 1st through hole 231 which connects the 1st-layer wiring 221 and the 2nd-layer wiring 222, and the 2nd through hole 232 which connects the 2nd-layer wiring 222 and the 3rd-layer wiring 223 at the intersection of the minimum grid made from the 2nd-layer wiring 222 and the 3rd-layer wiring 223, and it is constituted. Use 2nd-layer wiring 222, and the 1st-layer wiring 221 and since it constitutes, wiring in a hard macro wiring between hard macroes A hard macro top cannot be passed using the 1st-layer wiring 221 and the 2nd-layer wiring 222. Wiring was taken about to the empty field, without passing through a hard macro top, or the 3rd-layer wiring 223 was used only for the longitudinal direction of drawing, the hard macro top was passed, and it was wiring in the empty field after that by making it connect with the 1st-layer wiring 221 and the 2nd-layer wiring 222. Therefore, the shortest could not be wired, but wiring had to be taken about, and the wiring field was expanded and had the fault that area became large as the whole chip.
[0007] By using a multilayer interconnection, the purpose of this invention makes a wiring field small, and is to offer the semiconductor integrated circuit equipment which can reduce the area of the whole chip further.
[0008]
[Means for Solving the Problem] The hard macro which the semiconductor integrated circuit equipment of this invention connected between basic transistor components using the 1st-layer wiring and the 2nd-layer wiring which were prepared on the semiconductor integrated circuit, and was formed, The 3rd-layer wiring arranged in the longitudinal direction which connects between hard macroes, and the 4th-layer wiring arranged to the lengthwise direction which crosses perpendicularly to the 3rd-layer wiring and forms a grid, It has the 5th-layer wiring and the 6th-layer wiring which cross aslant, respectively and cross mutually to the 3rd-layer wiring and the 4th-layer wiring of those other than the intersection of the 3rd-layer wiring and the 4th-layer wiring.
[0009]
[Example] Next, this invention is explained with reference to a drawing.
[0010] Drawing 1 is a layout pattern for explaining one example of this invention.
[0011] In wiring for signal lines for connecting mutually the hard macro which connected between basic transistor components and was formed using the 1st-layer wiring and the 2nd-layer wiring which were prepared on the semiconductor chip, as shown in drawing 1 The 3rd-layer wiring 123 installed in the longitudinal direction on a drawing, and the 4th-layer wiring 124 arranged to the lengthwise direction on a drawing to the 3rd-layer wiring 123, It does not pass along the intersection of the 3rd-layer wiring 123 and the 4th-layer wiring 124, but the 5th-layer wiring 125 which crosses aslant, respectively and crosses mutually to the 3rd-layer wiring 123 and the 4th-layer wiring 124, and the 6th-layer wiring 126 are had and constituted. Moreover, the minimum grid made from the 3rd-layer wiring 123 and the 4th-layer wiring 124 is received. The 2nd-layer wiring 222 used within the hard macro by half-pitch gap **** of the 4th-layer wiring 124, On the intersection of the minimum grid which connected the 3rd-layer wiring 123 used for wiring between hard macroes in the 2nd through hole 132, and was made from the 3rd-layer wiring 123 and the 4th-layer wiring 124 In the minimum grid which connected the 4th-layer wiring 124 with the 3rd-layer wiring 123 in the 3rd through hole 133, and was made from the 3rd-layer wiring 123 and the 4th-layer wiring 124 by half-pitch gap **** of the 3rd-layer

wiring 123 In the minimum grid which connected the 5th-layer wiring 125 with the 4th-layer wiring 124 in the 4th through hole 134, and was made from the 3rd-layer wiring 123 and the 4th-layer wiring 124 like the 2nd through hole 132 by half-pitch gap **** of the 4th-layer wiring 124 The 5th-layer wiring and the 6th-layer wiring 126 are connected in the 5th through hole 135.

[0012] Drawing 2 is the layout pattern showing the 1st application of this invention.

[0013] When wiring connection is made from a lower output to the drawing vertical section input of the hard macro B on the drawing of the hard macro A according to the wiring pitch shown in drawing 1 as shown in drawing 2 , Carry out connection wiring of the 2nd-layer wiring 222 output which is wiring for signal lines in the hard macro A at the 3rd-layer wiring 123 using the 2nd through hole in the wiring field 13 linked to wiring between hard macroes, and connection wiring is carried out to the 4th-layer wiring 124 using the 3rd through hole 133. It connects with the 5th-layer wiring 125 using the 4th through hole 134 on the hard macro A. Wire to the drawing top lower right of the hard macro B, and connection wiring is carried out at the 4th-layer wiring 124 using the 4th through hole 134 on the wiring field 13. Using the 3rd through hole 133, connection wiring is carried out to the 3rd-layer wiring 123, and it connects with it at 2nd-layer wiring 222 input which is wiring for signal lines in the hard macro B using the 2nd through hole 132.

[0014] Drawing 3 is the layout pattern showing the 2nd application of this invention.

[0015] As shown in drawing 3 , when wiring connection is made from the drawing very best section output of the hard macro A to the drawing lower input of the hard macro B, Connection wiring is carried out at the 3rd-layer wiring 123 using the 2nd through hole 132 which connects to wiring between hard macroes 2nd-layer wiring 222 output which is wiring for signal lines in the hard macro A. Carry out connection wiring at the 4th-layer wiring 124 using the 3rd through hole 133, and connection wiring is carried out at the 5th-layer wiring 125 using the 4th through hole 134. Connect with the 6th-layer wiring 126 using the 5th through hole 135, and it wires to the hard macro B lower left. Carry out connection wiring at the 5th-layer wiring 125 using the 5th through hole 135, and connection wiring is carried out at the 4th-layer wiring 124 using the 4th through hole 134. Using the 3rd through hole 133, connection wiring is carried out and it connects with the 3rd-layer wiring 123 at 2nd-layer wiring 222 input which is wiring for signal lines in the hard macro B using the 2nd through hole 132.

[0016]

[Effect of the Invention] When the hard macro which this invention connected between basic transistors using the 1st-layer wiring and the 2nd-layer wiring on a semiconductor chip, and was formed as explained above is connected mutually, The 2nd through hole which connects the 2nd-layer wiring and the 3rd-layer wiring to the minimum grid which leading about of wiring was lost since the hard macro top was wired in the longitudinal direction, the lengthwise direction, and the direction of slant, and was made from the 3rd-layer wiring and the 4th-layer wiring, Since the 3rd through hole which connects the 3rd-layer wiring and the 4th-layer wiring, the 4th through hole which connects the 4th-layer wiring and the 5th-layer wiring, and the 5th through hole which connects the 5th-layer wiring and the 6th-layer wiring are arranged, wiring becomes possible in a comparatively short distance. The wire length which according to this example was 2 unit-length need conventionally in order to inherit two terminals with which an x-coordinate differs from a y-coordinate is 21/2. Since it becomes possible at a unit length Compared with a Prior art, a wiring field becomes small about 50% as an area, and conventionally, since the wiring field occupied about 60% of the chip area, it becomes possible [obtaining about 30% (=60%x0.5) of contraction as a chip area].

[0017] Thus, in this invention, a wiring field is made small and it has the effectiveness that contraction-ization of the whole chip can be obtained further.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The layout pattern for explaining one example of this invention.
[Drawing 2] The layout pattern showing the 1st application of this invention.
[Drawing 3] The layout pattern showing the 2nd application of this invention.
[Drawing 4] The layout pattern for explaining arrangement of the conventional wiring.
[Drawing 5] The layout pattern showing the 1st example of conventional semiconductor integrated circuit equipment.
[Drawing 6] The layout pattern showing the 2nd example of conventional semiconductor integrated circuit equipment.
[Description of Notations]
11 LSI Chip
13 Wiring Field
123,223 The 3rd-layer wiring
124 4th-Layer Wiring
125 5th-Layer Wiring
126 6th-Layer Wiring
132,232 The 2nd through hole
133 3rd through Hole
134 4th through Hole
135 5th through Hole
221 1st-Layer Wiring
222 2nd-Layer Wiring
231 1st through Hole
A, B Hard macro

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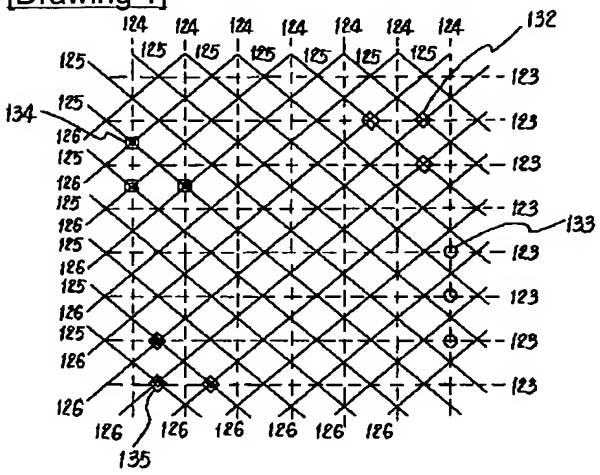
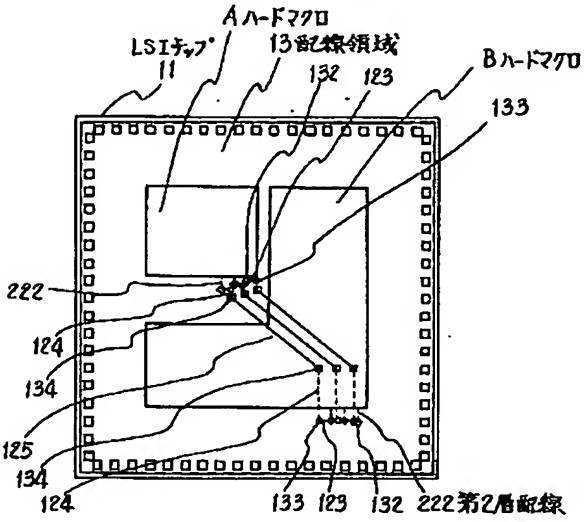
DRAWINGS

[Drawing 1]

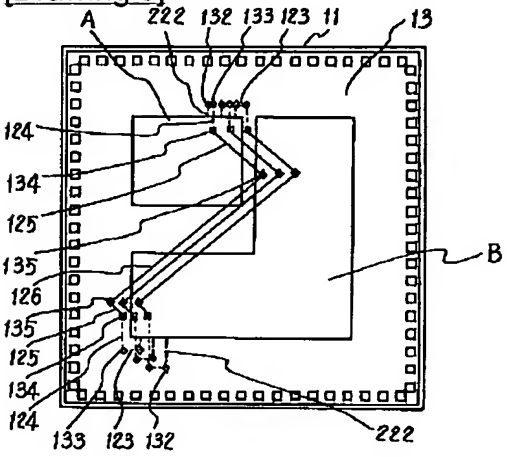


123：第3層配線　124：第4層配線
125：第5層配線　126：第6層配線
132：第2スルーホール　133：第3スルーホール
134：第4スルーホール　135：第5スルーホール

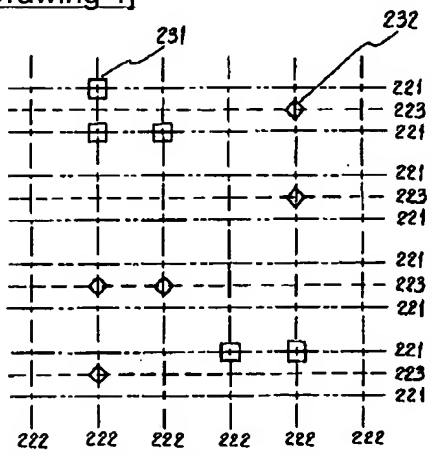
[Drawing 2]



[Drawing 3]

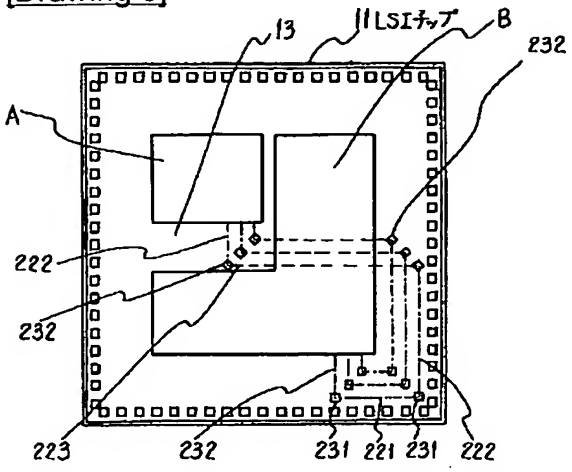


[Drawing 4]

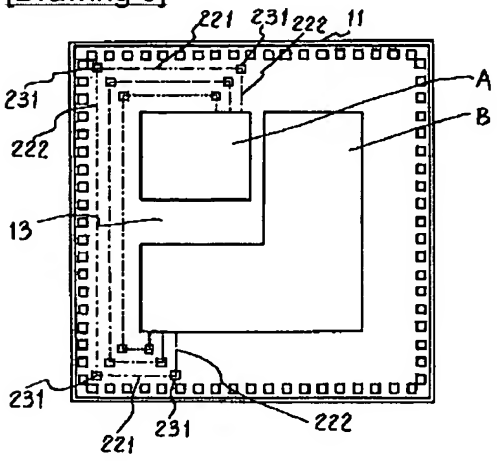


221: 第1層配線　222: 第2層配線
223: 第3層配線　231: 第1スルーホール
232: 第2スルーホール

[Drawing 5]



[Drawing 6]



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